Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously presented) A method for repairing defective memory elements using self-test circuitry in a memory having a plurality of memory elements including a first memory element and a second memory element, the method comprising:

counting fails in the first memory element with an on-chip logic counter;

counting fails in the second memory element with the on-chip logic counter;

comparing the number of fails in the first memory element to the number of fails in the second memory element;

determining the one of the first memory element and the second memory element having the most fails; and

allocating a redundant memory element to replace the one of the first memory element and the second memory element having the most fails.

2. (Original) The method of claim 1 further comprising counting fails in each additional memory element of the plurality of memory elements with the counter.

3. (Original) The method of claim 1 further comprising selectively associating each one of the plurality of memory elements with the counter and counting the fails in that memory element.

4. (Previously presented) The method of claim 2 wherein the memory includes a plurality of redundant memory elements, the method comprising allocating each one of the plurality of redundant memory elements to one of the plurality of memory elements having the most fails.

5. (Original) The method of claim 4 wherein the memory is identified as unrepairable when the number of memory elements having fails exceeds the number of redundant memory elements.

6. (Previously presented) The method of claim 1 wherein the redundant memory element replaces the first column or the second column only if one or more fails are counted in the first column or the second column.

7. (Original) The method of claim 1 wherein the plurality of memory elements include a plurality of columns and the redundant memory element includes a redundant column.

8. (Original) The method of claim 1 wherein the plurality of memory elements include a plurality of rows and the redundant memory element includes a redundant row.

9. (Original) The method of claim 1 wherein the plurality of memory elements includes a plurality of input/outputs and the redundant memory element includes a redundant input/output.

10. (Original) The method of claim 2 wherein the memory further comprises a second plurality of redundant memory elements perpendicular to the plurality of redundant memory elements, the method comprising designating one of the memory elements as a must fix memory element if a number of fails for that one of the memory elements exceeds a number of the second plurality of redundant memory elements available for allocation.

11. (Original) The method of claim 10 wherein the plurality of redundant memory elements includes columns and the second plurality of redundant memory elements includes rows.

12. (Original) The method of claim 1 further comprising allocating a perpendicular redundant memory element to repair any defects not repaired by the redundant memory element.

13. (Previously presented) A method according to claim 1 wherein the plurality of redundant memory elements include a plurality of columns and the redundant memory element includes a redundant column, the method further comprising:

testing the redundant column to determine a number of failing bits;

determining if the redundant column has less fails than one of the plurality of columns with the greatest number of failing bits; and

allocating the redundant column to replace the one of the plurality of columns with the greatest number of failing bits if the redundant column has fewer failing bits.

14. (Original) The method of claim 1 wherein the steps of the method are performed when power is applied to the memory.

15. (Canceled).

16. (Previously presented) An apparatus comprising:

a memory having a plurality of memory elements;

a redundant memory element suitable for replacing at least one of the plurality of memory elements;

a self-test circuit that tests the memory and allocates the redundant memory element to one of the plurality of memory elements if a defect is found, the self-test circuit including a multiplexer that selectively couples memory outputs to a fault counter that counts fails in each one of the plurality of memory elements tested by the self-test circuit;

a compare circuit that compares the number of fails in each of the memory elements and records the memory element having the most fails.

17. (Original) The apparatus of claim 16 further comprising a fault count storage that stores numbers of fails and address information for one or more memory elements containing fails detected during a self-test.

18. (Original) The apparatus of claim 16 wherein the plurality of memory elements include at least one of a row, a column, or an input/output.

19. (Original) The apparatus of claim 16 further comprising a second fault counter that counts fails in a second plurality of memory elements perpendicular to the plurality of elements, the second fault counter selectively coupled to memory outputs by a multiplexer.

20. (Original) The apparatus of claim 16 further comprising a reset signal provided to the fault counter after testing of each memory element.

21. (Original) The apparatus of claim 16 wherein the self-test circuit allocates one or more redundant rows after allocating at least one of redundant columns or redundant input/outputs.

22. (Original) The apparatus of claim 16, wherein the apparatus is provided within an embedded memory of an integrated circuit.

23. (Currently amended) An apparatus for ~~repairing~~ testing a memory, the apparatus comprising:

self-test circuitry for testing a plurality of memory elements, the self-test circuitry including a multiplexer, fault detection circuitry, and count compare circuitry,

the multiplexer selectively coupling an output from one of the plurality of memory elements to fault detection circuitry during a self-test, and

the count compare circuitry comparing the number of fails in each of the memory elements and recording the memory element having the most fails.

24. (Original) The apparatus of claim 23 wherein the fault detection circuitry includes an exclusive-or logic gate that compares a memory output to an expected memory output.

25. (Original) The apparatus of claim 23 wherein the fault detection circuitry includes a counter for counting fails within a memory element under test.

26. (Original) The apparatus of claim 25 wherein the self-test circuit provides a reset signal to the counter after testing each one of the plurality of memory elements.

27. (Original) The apparatus of claim 23 wherein the fault detection circuitry includes storage for storing fail data including a location of one of the memory elements and a number of fails detected for the one of the memory elements.

28. (Original) The apparatus of claim 23 wherein fault data is provided to an external device.

29. (Original) The apparatus of claim 28 wherein the fault data includes a full bit fail map.